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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/733,217	12/11/2003	Axel Brintzinger	2002 P 12234 US	8003

48154 7590 05/03/2007
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EXAMINER

THOMAS, TONIAE M

ART UNIT PAPER NUMBER

2822

MAIL DATE DELIVERY MODE

05/03/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/733,217	BRINTZINGER ET AL.	
	Examiner	Art Unit	
	Toniae M. Thomas	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
 - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
 - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
 - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 December 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 3,4,6,7,9-13 and 16-29 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 4,6,7,9-13,16-22,28 and 29 is/are allowed.
- 6) ☒ Claim(s) 3,23,24,26 and 27 is/are rejected.
- 7) ☒ Claim(s) 25 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 11 December 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>12/28/06</u> <u>1/11/07</u> | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This Office action is responsive to the amendment filed on 12 December 2006.
2. Currently, claims 3, 4, 6, 7, and 9-13, and 16-29 are pending.
3. The English translation of German Application DE 102 58 094.4 received on 28 December 2006 has perfected Applicant's claim to priority under 35 USC §119(a)-(d). Therefore, the Khandros et al. application publication (US 2004/0201074 A1) relied upon in the previous Office action mailed on 11 October 2006 is no longer available as prior art under 35 USC 102(e). Accordingly, the rejection, made of record in the previous action, of claims 3, 4, 7, 9-13, 16-26, and 28-29 under 35 USC §103(a) as being unpatentable over Khandros et al. in view of Klocke et al. (US 2003/0057093 A1) is withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Eldridge et al. (US 2001/0044225 A1). Rejections based on the Eldridge et al. reference follow.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary

skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. *Claims 3, 23-24 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eldridge et al. (US 2001/0044225 A1) in view of Klocke et al. (US 2003/0057093 A1)*¹.

Eldridge discloses a method of forming a plurality of three-dimensional structures on a substrate (see figs. 2A-2H and accompanying text). The method comprises the steps of: providing a wafer 32 with bumps 30 distributed on a surface of the wafer (fig. 2C and par. 0062, lines 1-3), wherein the bumps on the wafer comprise compliant elements (par. 0059, lines 1-15); and forming a resist 54 over the surface of the wafer including the bumps (fig. 2E and par. 0066, lines 1-7), wherein in one preferred embodiment the resist is formed by coating the surface of the wafer with an electrophoretic resist (par. 0066, lines 6-7). After forming the resist 54 over the surface of the substrate, the resist is patterned to expose a seed layer 52 (fig. 2F and par. 0068, lines 1-3), and a plurality of conductors 58 are formed over the exposed seed layer (fig. 2G and par. 0068, lines 7-10).

While Eldridge teaches forming the resist by coating the surface of the substrate with an electrophoretic resist, Eldridge does not explicitly teach forming the electrophoretic resist by: dipping the surface of the wafer into the

¹ The Klocke et al. application publication was relied upon in the previous action mailed on 11 October 2006.

electrophoretic resist; and applying an electrical voltage between the wafer and the electrophoretic resist.

The Klocke et al. application publication (referred to hereinafter as Klocke) discloses a method of depositing an electrophoretic resist on microelectronic workpieces (par. 9, lines 10-14). The electrophoretic resist is formed by: placing a workpiece into an electrophoretic resist; applying an electrical voltage between the substrate and the electrophoretic resist, while the workpiece is in the electrophoretic resist; and subsequently removing the workpiece from the electrophoretic resist (fig. 17; par. 091, lines 1-19; and par. 0111, lines 1-3). The method further comprises heating the workpiece after removing the workpiece from the electrophoretic resist (par. 112, lines 8- 18).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to coat the surface of the wafer with an electrophoretic resist using the method taught by Klocke, because: an electrophoretic resist formed using the method of Klocke conforms uniformly to the surface of the wafer despite the uneven topography on the surface of the wafer created by the compliant elements.

5. *Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Eldridge in view of Klocke as applied to claim 3 above, and further in view of Brooks et al. (US 6,084,297).²*

² The Brooks et al. patent was relied upon in the previous Office action mailed on 11 October 2006.

As discussed above, Eldridge discloses forming a plurality of conductors 58 over that portion of the seed layer 52 not covered by the resist 54, wherein in one preferred embodiment the plurality of conductors may comprise a gold layer overlying a nickel layer (par. 0069, lines 12-18). However, Eldridge does not disclose forming a copper layer over the uncovered portion of the seed layer, and sequentially forming a nickel layer and a gold layer over the copper layer.

The Brooks et al. patent (referred to hereinafter as Brooks) discloses forming a plurality of conductors 32 (fig. 1 and col. 5, lines 46-49). The plurality of conductors comprises a copper layer, a nickel layer formed over the copper layer, and a gold layer formed over the nickel layer (col. 5, lines 50-53).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the combination of Eldridge and Klocke by forming a copper layer over the uncovered portion of the seed layer prior to forming the nickel layer, as taught by Brooks, since copper has excellent conductivity and can be selectively deposited onto the uncovered portion of the seed layer using an electroplating method.

Allowable Subject Matter

6. Claim 25 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the

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limitations of the base claim and any intervening claims. Also, claims 4, 6-7, 9-13, 16-22, and 28-29 are allowable over the prior art of record.

7. The prior art of record fails to anticipate, teach or suggest - either separately or combined - a method for forming a plurality of three-dimensional structures on a wafer substantially as claimed, wherein the method comprises forming a plurality of conductors, which electrically couple (or connect) a pad formed on the wafer to a terminal either on the surface of the wafer or on the bump.

8. The amendment received on 28 December 2006 has overcome the following objection and rejection made of record in the previous Office action mailed 11 October 2006: the objection to claims 23-25 for minor informalities not affecting the scope of the claims, and the rejection of claim 28 under 35 USC §112, second paragraph. Accordingly, the objection and rejection are withdrawn.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toniae M. Thomas whose telephone number is (571) 272-1846. The examiner can normally be reached on Monday through Friday from 8:30 a.m. to 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

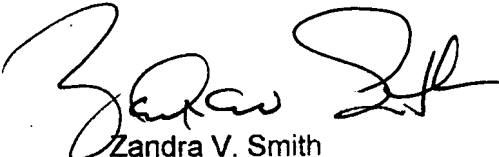
Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see

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<http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TMT

26 April 2007



Zandra V. Smith
Supervisory Patent Examiner
27 April 2007